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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/697,357 | 10/29/2003 | Viswanathan Lakshmanan | 03-1772 81610 | 7491 |

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| EXAMINER | |
|---|---|
| DOAN, NGHIA M | |
| **ART UNIT** | **PAPER NUMBER** |
| 2825 | |

DATE MAILED: 03/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/697,357 | LAKSHMANAN ET AL. | |
| | Examiner | Art Unit | |
| | Nghia M. Doan | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7,8 and 14* is/are rejected.

7)☒ Claim(s) *2-6,9-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Responsive to communication application 10/697,357 filed on 10/29/2003, claims 1-14 are pending in this Office Action.

### *Drawings*

2. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated (see page 3, lines 23-24 of applicant's specification). See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Specification*

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The abstract of the disclosure is objected to because states that Abstract lacks narrative format and merely paraphrase to claim 1. Correction is required. See MPEP § 608.01(b).

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**6. Claims 1, 7, 8, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Teh et al. (Teh) (US 2002/0138813).**

7. **With respect to claims 1 and 8**, Teh discloses a method and computer program product for partitioning an integrated circuit design for physical design verification (Abstract) comprising:

(claim 8) a medium for embodying a computer program for input to a computer (Abstract, system); and

(claim 8) a computer program embodied in the medium for causing the computer to perform (Abstract, command file) steps of:

(claims 1 and 8) (a) receiving as input a representation of an integrated circuit design having a number of physical design layers (figures 4, 5, and 6B – number of physical layer such as: logic layer, memory layer; page 3, ¶ 31, col. 2, ll. 1-3 and ¶33-¶34);

(claims 1 and 8) (b) receiving as input a composite run deck specifying rule checks to be performed on the integrated circuit design (figures 4, 5, and 6A –rule checker such as: logic rule, memory rule --; page 3, ¶ 29, ll. 1-7 and ¶33);

(claims 1 and 8) (c) partitioning (separating/dividing) (Abstract) the composite run deck into partitioned run decks so that the number of physical design layers referenced by each of the partitioned run decks is a minimum (Abstract, figures 4, 5, 6A, and 6B–page 3, ¶ 29, ll. 14-26, ¶30-¶33, and page 4, ¶38);

(claims 1 and 8) (d) parsing the representation of the integrated circuit design to filter only the physical design layers required for each of the partitioned run decks into a filtered data deck for each of the partitioned run decks (--ensuring that design rule checker is able to correlate a particular region in a layer with a particular set of design rules) (Abstract, figures 4, 5, 6A, and 6B–page 3, ¶32-¶34, and page 4, ¶38); and

(claims 1 and 8) (e) generating as output (result) the filtered data deck for each of the partitioned run decks (page 4, ¶37-¶38).

8. **With respect to claim 7 and 14**, Teh discloses the limitations of claims are depended, wherein the representation of the integrated circuit design is a Graphic Data System stream format file (¶04, ¶10, ¶29, ¶31, claim 9).

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. **Claims 1, 7, 8, and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Richardson et al. (Richardson) (US 6,606,735).**

11. **With respect to claims 1 and 8**, Richardson discloses a method and computer program product for partitioning an integrated circuit design for physical design verification (Abstract) comprising:

(claim 8) a medium for embodying a computer program for input to a computer (col. 12, ll. 20-42, col. 14, ll. 17-26, and col. 16, ll. 55-64); and

(claim 8) a computer program (instruction code) embodied in the medium for causing the computer to perform (co. 4, ll. 63-67; col. 12, ll. 1-10) steps of:

(claims 1 and 8) (a) receiving as input a representation of an integrated circuit design having a number of physical design layers (col. 6, ll. 33-53);

(claims 1 and 8) (b) receiving as input a composite run deck specifying rule checks to be performed on the integrated circuit design (col. 4, ll. 63-67; col. 5, ll. 36-50) and col. 6, ll. 5-19);

(claims 1 and 8) (c) partitioning (dividing) the composite run deck into partitioned run decks so that the number of physical design layers referenced by each of the partitioned run decks is a minimum (col. 4, ll. 26-40);

(claims 1 and 8) (d) parsing the representation of the integrated circuit design to filter only the physical design layers required for each of the partitioned run decks into a filtered data deck for each of the partitioned run decks (col. 2, ll. 42-50, col. 4, ll. 35-53, col. 6, ll. 37-67, col. 7, ll. 1-4); and

(claims 1 and 8) (e) generating as output the filtered data deck for each of the partitioned run decks (col. 6, ll. 42-53 and ll. 62-67).

12. **With respect to claim 7 and 14**, Richardson discloses the limitations of claims are depended, wherein the representation of the integrated circuit design is a Graphic Data System stream format file (col. 2, ll. 61-67, and col. 12, ll. 59-67).

***Allowable Subject Matter***

13. Claims 2-6 and 9-13 are objected to as being dependent upon a rejected base claim, but would be allowable if claims 2 and 9 are rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter: As per claims 2-6 and 9-13, the prior art in the record does not teach or fairly suggest the further limitations of the claims 2 and 9 from which the respective claims depend comprising the inventive step of determining a memory size required to run each filtered data deck on a physical design verification processor from the filtered data deck for each of the partition run decks. In particular, Ho (US 6,378,110) discloses a method verification a physical layout, which is including a number of physical layers associated with pre-determined a set of rules for reducing amount of memory and time development for verification process (Abstract, and col. 5, ll. 1-35); and Tetrick et al. (US 5,768,585) discloses a microprocessor subsystem for sharing memory are allocated to each of the processors for reducing amount of memory and time development required (Abstract, figure 1, and col. 2, ll. 5-17). Moreover, none of the prior arts made of record teach or suggest the inventive steps as claimed.

***Conclusion***

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NMD

Nghia M. Doan
Patent Examiner
AU 2825
NMD

PHALLAKA KIK
U.S. PATENT EXAMINER